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EXAMINER	
TRAN, NHAN T	

ART UNIT	PAPER NUMBER
2615	14

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/901,280	Applicant(s) ROSSI ET AL.	
	Examiner Nhan T. Tran	Art Unit 2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *1/22/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/22/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1 - 34 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 7-11, 13-34 are rejected under 35 U.S.C. 102(e) as being anticipated by Nair et al (US 6,366,320).

Regarding claim 1, Nair discloses an apparatus comprising:

groups of image sensors (one group corresponds to each multiplexer 130 to 179 of first level multiplexing), each group comprising subgroups (columns) of sensors (see Fig. 1; col. 1, lines 10-29; col. 3, lines 48-56, wherein the storage array 110 is also a sensor array);

subgroup select circuits (gate pairs in multiplexers 130 to 179), each of which is coupled to outputs from a respective subgroup of sensors (see Fig. 1; col. 3, lines 44-56);

group select circuits (gate pairs in multiplexers 180 to 186), each of which is coupled to outputs from subgroup select circuits associated with a respective one of the groups (Fig. 1);

a first bus for each group coupled to the outputs of the associated subgroup select circuits (i.e., a bus between 130 and 180; Fig. 1);

a controller (192) for providing control signals to the subgroup select circuits and the group select circuits to selectively enable the respective subgroup select circuits and group select circuits to pass signals from the sensors to a readout circuit (122, 126) one sensor at a time (sequential outputting/multiplexing of pixel by pixel, column by column) as shown in Fig. 1; col. 3, line 48 – col. 4, line 25;

an isolation circuit (each gate pair in multiplexers 180 to 186) coupled to each first bus for selectively isolating each group from the readout circuit (by turning on and then off each gate pair of multiplexers 180 to 186 in column by column basis; Fig. 1; col. 3, line 48 – col. 4, line 25).

Regarding claim 2, Nair also refers that the sensors are active pixel sensors (col. 1, lines 16-20).

Regarding claim 3, Nair further discloses a second bus coupled to the outputs of the group select circuits and the readout circuit (i.e., a bus between 180 and 187 that is coupled to the readout circuit 122, 126 via 187).

Regarding claim 4, Nair discloses that the number of group select circuits is approximately equal to the square root of the number of the subgroup select circuits (col. 4, lines 3-10, wherein 7 second level muxes ≅ square root of 50 first level muxes).

Regarding claim 7, in col. 4, lines 3-10 and Fig. 1, Nair discloses that the 32 predetermined coded lines selects one of 16 pass gate pairs in the selected first level mux, a corresponding one of 8 pass gate pairs in the selected second level mux, and finally a corresponding one of 8 pass gate pairs in the third level mux. It is implied that when one gate pair in the multiplexer 180 corresponding to the 16 gate pairs in the multiplexer 130 is **ON**, the 16 gate pairs are also sequentially **ON** to pass the signals from the 16 gate pairs to the first bus between the 130 and 180 for the multiplexers sequentially output signals. When the signals output from the 16 gate pairs are done, the corresponding gate pair in the multiplexer 180 must be **OFF** and a next gate pair of the 8 gate pairs in the multiplexer 180 is **ON** to sequentially receives output signals from the next corresponding 16 gate pairs (i.e., 131) and so on. Thus, each group select circuit of 180 comprises at least a transistor switch with a respective gate terminal (either a full CMOS gate or a half gate) for receiving a control signal from the controller (192), wherein when the switch is turned on, the group select circuit is enabled to pass signals from associated subgroup select circuits to the first bus, and when the switch is turned off, the group select circuit is disabled from passing signals from the associated group select circuits to the first bus.

Regarding claim 8, see the analysis in claim 7 for the similar structure and operations of each subgroup select circuit.

Regarding claim 9, Nair discloses that the controller (192) is configured for generating the control signals (by decoding 10 bit column address) to enable and disable the group select circuit switches and the subgroup select circuit switches in a predetermined sequence (col. 3; line 57 – col. 4, line 10 and note that a predetermined sequence is pixel by pixel in column by column basis as described in col. 3, lines 42-46).

Regarding claim 10, Nair also discloses that the controller is configured to provide the control signals to enable the switches in the group select circuits sequentially, and, while a particular group select switch is enabled, to enable the subgroup select circuits associated with the particular group select circuit sequentially, one at a time (Fig. 1; col. 4, lines 3-10 and the Examiner's analysis in claims 1, 7 & 9 are also applied here).

Regarding claim 11, see the analysis in claim 9.

Regarding claim 13, Nair further discloses supergroups of sensors (all sensors corresponding to each multiplexer 180 to 186; Fig. 1);

supergroup select circuits (gate pairs in multiplexer 187), each of which is coupled to outputs from group select circuits associated with respective one of the supergroups;

wherein the controller is configured to provide control signals to the supergroup select circuits to selectively enable a supergroup select circuit to pass a signal from the second bus to a third bus (i.e., a bus between 187 and 122) which is a common output bus (see Fig. 1 and the Examiner's analysis in claims 1, 3, 7 & 9).

Regarding claim 14, it is shown in Fig. 1 at multiplexer 187 that an output of each supergroup select circuit is coupled electrically to a common output bus.

Regarding claim 15, see claim 7 for the similar analysis for a transistor switch with a respective gate terminal for receiving a control signal from the controller.

Regarding claim 16, Nair discloses a method comprising:

selectively enabling a group select circuit (i.e., each gate pair of multiplexer 180) to electrically couple a charge mode read-out amplifier (at 126; col. 4, lines 22-24) to a respective set of subgroup select circuits (i.e., multiplexer 130) as shown in Fig. 1; col. 4, lines 3-10. It is noted that the amplifier at 126 is also considered as a charge mode read-out amplifier since it amplifies the signal charges from the sensor array during reading out.

when the group select circuit is enabled, enabling a pixel output signal to pass from each subgroup select circuit of the respective set of subgroup select circuits in a sequential manner through the group select circuit to the charge mode read-out amplifier, subsequently disabling the group select circuit to electrically isolate the charge mode read-out amplifier from the respective set of subgroup select circuit. See col. 3, line 47 – col. 4, line 10, wherein each gate pair of

multiplexer 180 operates to switch on and then off (bus by bus basis) to isolate signal charges output from multiplexer 130 and the amplifier at processing pipe 126 via multiplexer 187 and then from multiplexer 131 and the amplifier and so on in sequential manner to produce a pixel signal chain at the output of multiplexer 118.

Regarding claim 17, see the analysis in claim 16 for the same operation for another group select circuit and respective set of subgroup select circuits (i.e., multiplexer 131).

Regarding claim 18, see the analysis in claim 16, wherein each gate pair in multiplexers 180-186 corresponding to each first level multiplexing at 130-179 is sequentially disabled to produce a pixel signal chain.

Regarding claim 19, see the analysis in claim 16. Furthermore, a supergroup select circuit is represented by each gate pair in the multiplexer 187 as shown in Fig. 1.

Regarding claims 20 - 23, see the analysis in claims 17 & 18 for the similar operations at the third level of multiplexing at 187 and in combination with the second and first level of multiplexing (col. 4, lines 3-10).

Regarding claim 24, inherent in the transmission gate disclosed in col. 3, lines 52-56 is a voltage source connected to the gate.

Regarding claim 25, see the analysis in claim 1.

Regarding claim 26, Nair discloses the step of amplifying the readout signals from the array (col. 4, lines 22-25).

Regarding claim 27, as shown in Fig. 1 and col. 3, lines 48 – col. 4, line 10, a low voltage that is sufficient to disable (turn off) the transmission gate must be applied to the non-enabled groups in order for the multiplexing operation to function as disclosed.

Regarding claim 28, see the analysis in claim 13.

Regarding claim 29, Nair clearly discloses a step of coupling each group select circuit to an associated differential bus, wherein the readout signals from each sensor in the group will travel through the bus (see Fig. 1 and col. 3, lines 48-56).

Regarding claim 30, it is inherent in Nair in that a predetermined reference voltage at each bus for producing a differential, non-destructive readout of the sensors must be maintained for the multiplexing operation to function properly.

Regarding claim 31, see the analysis in claim 1 and Fig. 1, wherein each group comprises a plurality of columns of an image sensor array, and a plurality of column select circuits, each of which coupled to an output from a column of sensors (col. 3, lines 48-56).

Regarding claim 32, see the analysis in claim 2.

Regarding claim 33, see the analysis in claim 1.

Regarding claim 34, see the analysis in claims 1 & 13.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 5, 6, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nair et al (US 6,366,320).

Regarding claims 5 & 6, although Nair does not specifically disclose that a ratio of the number of subgroup select circuits to group select circuit is in a range of 15:1 and 30:1 as required in claim 6 (this is also within the range of 10:1 and 40:1 required in claim 5), Nair suggests, in col. 1, lines 29-37, that modern imaging arrays can be very large and future arrays are expected to be even larger which requires modification on circuit design. Therefore, it would

have been obvious to one of ordinary skill in the art to implement a ratio of the number of subgroup select circuits to group select circuit in a range of 10:1 and 15:1 as an obvious variation depending on the actual size of the sensor device.

Regarding claim 12, although Nair does not clearly disclose that each group select circuit comprises a pair of NMOS transistor switches, Nair suggests that each pair can be a full CMOS transmission gate (comprises a complementary pair of a NMOS and a PMOS transistor), a half gate (either a pair of PMOS transistors or a pair of NMOS transistors) or any other device that acts as a switch (col. 3, lines 52-56).

Therefore, it would have been obvious to one of ordinary skill in the art to implement the switches by using NMOS switches instead of a full CMOS switches in view of the suggestion of Nair in an obvious configuration for the transmission gates.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (703) 605-4246. The examiner can normally be reached on Monday - Thursday, 8:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew B Christensen can be reached on (703) 308-9644. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NT.

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